REMARKS

In response to the Office Action dated November 21, 2002, Applicant has amended claims 3, 19, and 20 to more appropriately claim his invention and added claims 21-25 to protect additional aspects thereof. Please consider the following remarks.

In the Office Action, claims 3, 12, 13, 19 and 20 were rejected under 35 U.S.C. § 112, second paragraph. Additionally, claims 3, 12, 13 and 19 were rejected under 35 U.S.C. § 102 (e) as being anticipated by U.S. Pat. No. 6,239,495 to Sakui et al. ("Sakui"). Also, claim 20 was rejected under 35 U.S.C. § 103(a) as obvious over Sakui in view of U.S. Pat. No. 6,236,109 to Hsuan et al. ("Hsuan"). These rejections are respectfully traversed for the following reasons.

Rejections Under 35 U.S.C. §112

The Examiner rejected claims 3, 12, 13, 19, and 20 under 35 U.S.C. § 112 because the term "semiconductor element" is not clear. The Examiner states that "the specification page 12, lines 3-8, discloses 'a semiconductor element' recited in claims as an internal circuit built in a wiring substrate in Fig. 1." (Office Action page 2). We believe the Examiner has misunderstood the disclosure on page 12 of the specification. The portion of the specification cited by the Examiner does not mean that the semiconductor element is part of the *wiring substrate*. Instead, that the semiconductor element (internal circuit) is formed on the formation surface 2 of the *semiconductor chip* 1. Thus, contrary to the Examiner's assertion, the meaning of semiconductor element in the specification is consistent with the use of the term in the claims and is thus clear.

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Nonetheless, to clarify the meaning of the term semiconductor element, Applicant has amended the specification at page 12, lines 3-8. Because the amendment simply clarifies the original meaning of the sentence as filed, it does not add any new matter. Therefore, because the meaning of semiconductor element as used in the claims is clear, the rejection of claims 3, 12, 13, 19 and 20 under § 112 should be withdrawn.

The Examiner also rejected claim 19 under 35 U.S.C. § 112, second paragraph because the recitation of the conductive bumps in claim 19 "does not make sense." In response, Applicant has amended claim 19 to recite a "semiconductor device according to claim 12, wherein said at least portion of the plurality of connecting terminals are conductive bumps." Such amendment finds support in the application as originally filed and adds no new matter. As result, the rejection of claim 19 under § 112 should be withdrawn.

Rejections Under 35 U.S.C. § 102(e)

Claims 3, 12, 13, and 19 were rejected under 35 U.S.C. § 102(e) as being anticipated by Sakui. Sakui does not anticipate claims 3, 12, 13, and 19 because it fails to disclose each and every feature recited by the claims.

To properly anticipate the claims under § 102, Sakui, taken alone, must disclose each and every feature recited by the claims. In this case, however, Sakui fails to disclose each and every feature of the rejected claims. For example, Sakui fails to disclose at least a semiconductor device having one of the first connecting terminals and the second connecting terminals arranged to be facing to the assembly board and the average density of arrangement of the one of the first connecting terminals and the

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second connecting terminals are made lower than that of another of the first connecting terminals and the second connecting terminals, as recited by independent claim 3. Because Sakui does not disclose at least this feature of claim 3, it does not anticipate the claim. Moreover, claims 12, 13, and 19 are allowable at least by virtue of their dependence from allowable independent claim 3. As a result, the rejection of claims 3, 12, 13, and 19 under § 102 as anticipated by Sakui should be withdrawn and the claims allowed.

Rejections Under 35 U.S.C. § 103(a)

Claim 20 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Sakui in view of Hsuan. The Examiner alleges that Sakui discloses all features recited by claim 20, except that Sakui does not disclose features related to the size of the first and second chips. The Examiner asserts, however, that FIG. 6A of Hsuan provides the teaching of a multi-chip packaging device wherein the second semiconductor chip is larger than the first semiconductor chip. The rejection of claim 20 is respectfully traversed because the Examiner has failed to establish a *prima facie* case of obviousness.

One of the requirements for establishing a *prima facie* case of obviousness is that the references, taken alone or in combination, must teach or suggest each and every feature recited by the claims. In this case, however, Sakui and Hsuan, taken alone or in combination, fail to teach or suggest each and every feature recited by claim 20. For example, the cited references fail to teach or suggest at least a semiconductor device having one of the first connecting terminals and the second connecting terminals

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arranged to be facing to the assembly board and the average density of arrangement of the one of the first connecting terminals and the second connecting terminals are made lower than that of another of the first connecting terminals and the second connecting terminals, as recited by claim 20. Because the references fail to teach or suggest at least these features, the rejection of claim 20 should be withdrawn and the claim allowed.

New Claims 21-25

Applicants have added claims 21-25 to protect additional features of the invention. These claims find support throughout the specification and therefore add no new matter. Each of the new claims recites features not taught or suggested by the prior art of record.

Independent claim 21 recites a semiconductor device comprising a first semiconductor chip where a semiconductor element is formed; a plurality of first connecting terminals arranged on a semiconductor element formation surface side in the first semiconductor chip, and connected electrically to the semiconductor element; conductive members buried in a plurality of through holes that go through the first semiconductor chip; and a plurality of second connecting terminals arranged on a back surface side of the semiconductor element formation surface in the first semiconductor chip, and connected electrically to the semiconductor element via the conductive members, wherein at least either the first connecting terminals or the second connecting terminals is coupled to an assembly board, and a portion of either the first connecting terminals or the second connecting terminals are distributed and arranged on the

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central area of the semiconductor chip, and power source supply potential or ground potential are to be applied thereto. Claim 21 is allowable because it recites features not taught or suggested by the prior art of record. Furthermore, claims 22-24 are allowable at least by virtue of their dependence from allowable claim 21.

Claim 25 recites a semiconductor device comprising a first semiconductor chip where a semiconductor element is formed; a first connecting terminal arranged on a semiconductor element formation surface side in the first semiconductor chip, and connected electrically to the semiconductor element; a conductive member buried in a through hole that goes through the first semiconductor chip; a second connecting terminal arranged on a back surface side of the semiconductor element formation surface in the first semiconductor chip, and connected electrically to the semiconductor element via the conductive member; a second semiconductor chip stacked on the first semiconductor chip; a third connecting terminal arranged on a semiconductor element formation surface side in the second semiconductor chip, wherein one of the first connecting terminal and the second connecting terminal of the first semiconductor chip is arranged at a position facing to the third connecting terminal of the second semiconductor chip, the first semiconductor chip and the second semiconductor chip are electrically connected with each other through the facing connecting terminals, the second semiconductor chip is thicker or larger than the first semiconductor chip, and a portion of either the first connecting terminals or the second connecting terminals are distributed and arranged on the central area of the semiconductor chip, and power source supply potential or ground potential are to be applied thereto. Claim 25 is allowable because it recites features not taught or suggested by the prior art of record.

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Conclusion

In view of the foregoing, Applicant respectfully requests the reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P.

Dated: February 21, 2003

By: Reg 24,014
for Richard V. Burgujian
Reg. No. 31,744

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APPENDIX TO AMENDMENT

VERSION WITH MARKINGS TO SHOW CHANGES MADE

AMENDMENTS TO THE SPECIFICATION

Beginning on page 12, line 3 and continuing on page 13, lines 1-4, please amend the paragraph as follows:

In FIG. 1A, a semiconductor chip 1 is mounted [onto] on a wiring substrate 7 through a conductive bump 4 so that a formation surface 2 of the semiconductor chip 1 on which a semiconductor element (internal circuit) is formed faces to [the] a surface of the chip 1 side of the wiring substrate 7, which surface is on the side of the semiconductor chip 1, namely the semiconductor chip 1 is mounted on the wiring substrate 7 in face-down status. Connecting terminal (conductive bump) 4 being distributed over the entire area (for example, in an array shape) are formed on the formation surface 2 of the semiconductor element. The wiring substrate 7 comprises an insulated substrate main body 7A made of resin or the like, and a wiring layer (multi layer wiring) 7B is formed on the surface of the chip 1 side, the back surface and the inside of the wiring substrate 7. The bump 4 is arranged on the surface of the semiconductor element formation surface 2 side of the semiconductor chip 1 corresponding to the wiring layer 7B on the surface of the chip 1 side of the wiring substrate 7, and the semiconductor element formation surface 2 of the semiconductor chip 1 is electrically connected through the bump 4 to the wiring layer 7B of the wiring

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substrate 7. The wiring layer 7B on the surface of the chip 1 side of the wiring substrate 7 is also communicated to a wiring layer 7B arranged in the wiring substrate 7 and derived to the back surface side of the wiring substrate 7, and is electrically connected to a connecting terminal (conductive bump) 13 arranged on the back surface of the wiring substrate 7 for connection to a mother board.

AMENDMENTS TO THE CLAIMS

Please amend claims 3, 19 and 20 as follows:

3. (Amended) A semiconductor device comprising:

a first semiconductor chip where a semiconductor element is formed;

a plurality of first connecting terminals arranged on a semiconductor element formation surface side in the first semiconductor chip, and connected electrically to the semiconductor element;

conductive members buried in a plurality of through holes that go through the first semiconductor chip; and

a plurality of second connecting terminals arranged on a back surface side of the semiconductor element formation surface in the first semiconductor chip, and connected electrically to the semiconductor element via the conductive members[;] ,

wherein[,] at least either the first connecting terminals or the second connecting terminals is coupled to a assembly board[.] , and

one of the first connecting terminals and the second connecting terminals are arranged to be facing to the assembly board and the average density of arrangement of the one of the first connecting terminals and the second connecting terminals is lower

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than that of another of the first connecting terminals and the second connecting terminals.

19. (Amended) A semiconductor device according to claim 12, [further comprising a conductive bump configured to connect] wherein said at least a portion of the plurality of connecting terminals [of the semiconductor chips to be stacked with each other] comprises conductive bumps.

20. (Amended) A semiconductor device comprising:

a first semiconductor chip where a semiconductor element is formed;

a first connecting terminal arranged on a semiconductor element formation surface side in the first semiconductor chip, and connected electrically to the semiconductor element;

a conductive member buried in a through hole that goes through the first semiconductor chip;

a second connecting terminal arranged on a back surface side of the semiconductor element formation surface in the first semiconductor chip, and connected electrically to the semiconductor element via the conductive member;

a second semiconductor chip stacked on the first semiconductor chip;

a third connecting terminal arranged on a semiconductor element formation surface side in the second semiconductor chip[;] ,

wherein[,] one of the first connecting terminal and the second connecting terminal of the first semiconductor chip is arranged at a position facing to the third

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connecting terminal of the second semiconductor chip, the first semiconductor chip and the second semiconductor chip are electrically connected with each other through the facing connecting terminals, [and]

the second semiconductor chip is thicker or larger than the first semiconductor chip[.] , and

one of the first connecting terminals and the second connecting terminals are arranged to be facing to the assembly board and the average density of arrangement of the one of the first connecting terminals and the second connecting terminals is lower than that of another of the first connecting terminals and the second connecting terminals.

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